FIG. 1
(PRIOR ART)

FIG. 2
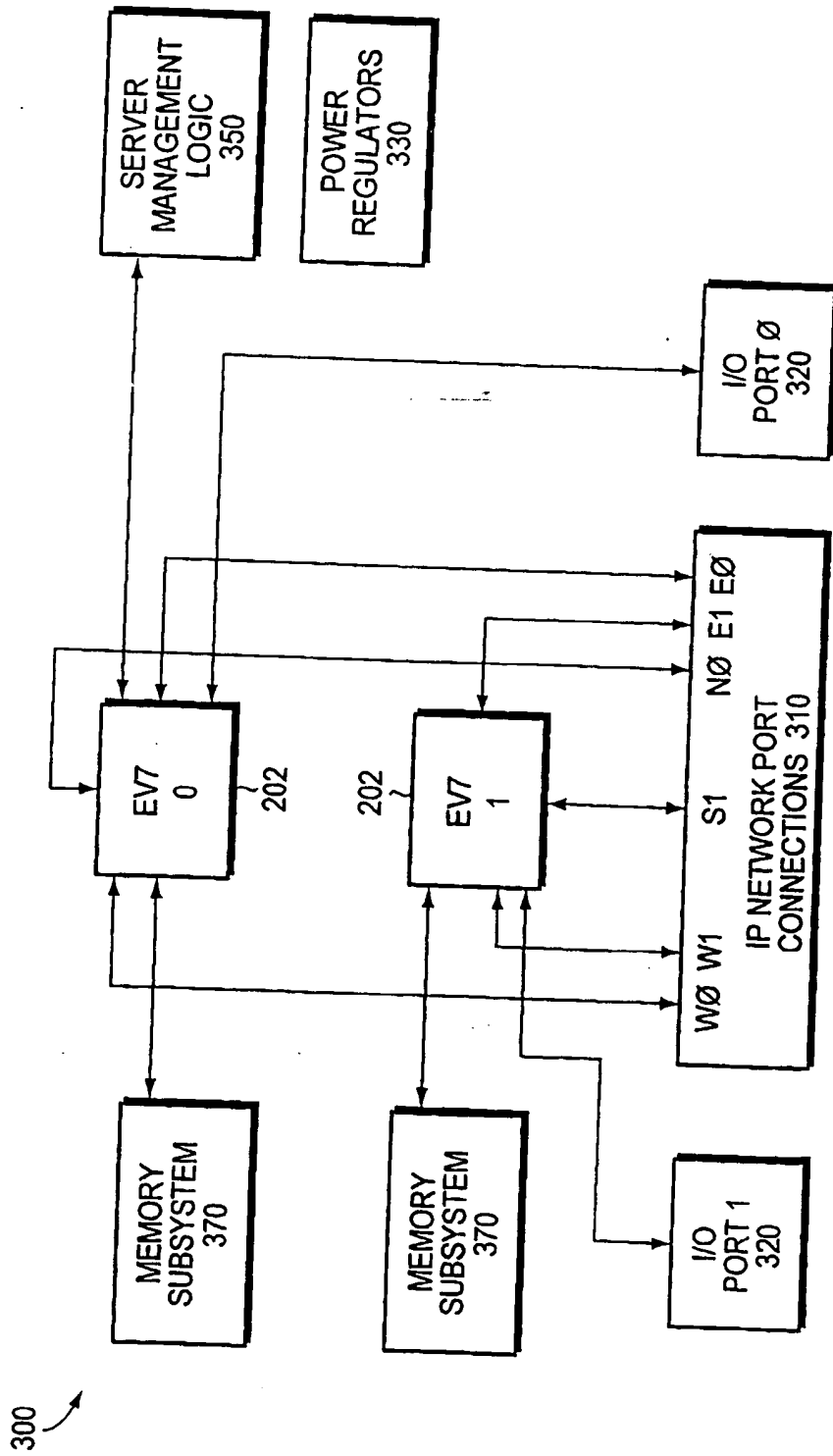
FIG. 3
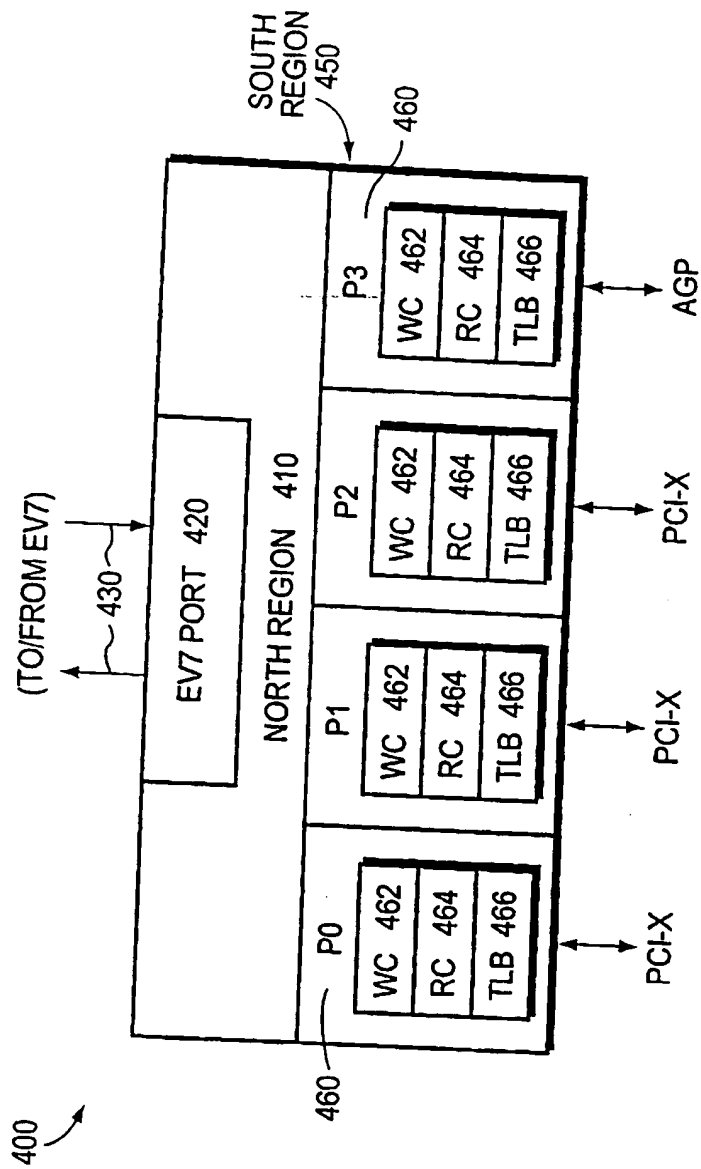
FIG. 4
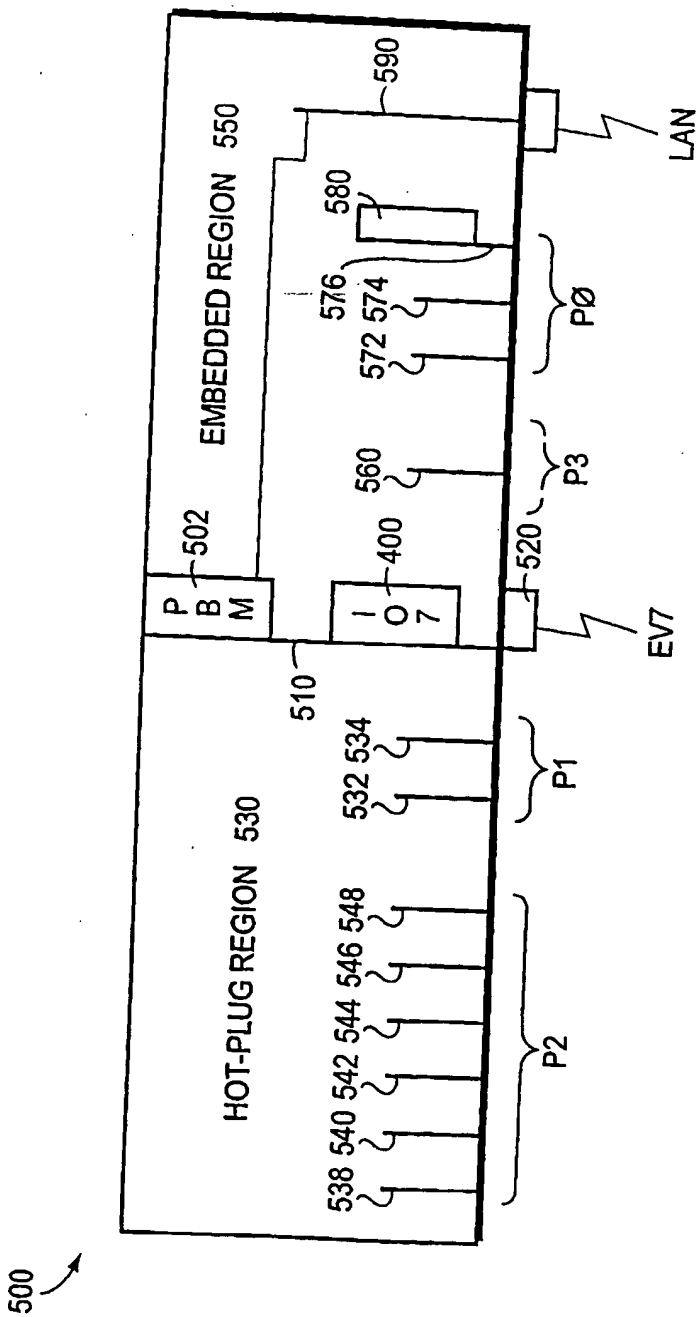
FIG. 5
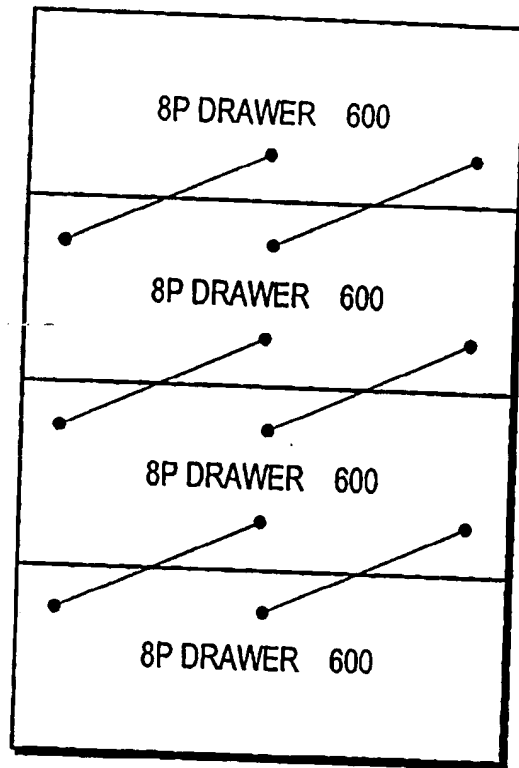
FIG. 6

FIG. 27

FIG. 8

EV7 up hose

EV7 down hose

[uph]

[dnh]

[mux]

Port 7 [sp7]
Port 0 [sp0]
Port 1 [sp1]
Port 2 [sp2]
Port 3 [sp3]

up hose resp done
up hose packet type
msi to Port 7
up hose address / header
up hose data
down hose data
down hose address
down hose unordered packet-type
down hose ordered packet-type
down hose packet done

TLB data

00	0
01	1
02	2
03	3
04	
05	
06	
07	
08	
09	
10	
11	

up hose ordering engine

[upe]

TLB block [tlb]

down hose forward initiator [dfi]

mask

error

up hose data [wbf]

8b x 192w

64b x 224w

south port control bits

south port errors and status

Pins for Hot Plug

IO7 Internal CSR data [csr]

Hot Plug [hplg]

down hose data [rbf]

66b x 224w

down hose add [dna]

82b x 8w

down hose ordering engine [dne]

FWD address

up data

down data

down address

Rsp hdr

agp/pci_addr_in

addr_in

down data

pci_addr_out

csr_data from csr,tlb,hplg

pci_data_in

addr_in

AGP [agp]

PCI/PCI-X [pcx]

AGP_sba_in   AGP_ad_in   AGP_ad_out

PCI_ad_in   PCI_ad_out

FIG. 9

PO x_ CTRL

Name	Extent	Access	Initial State	Firmware Init'ed State	
CACHE_LINE_LEN	7:0	RW	40	*Must Be* 40	Cache line size. Used by Megacell for PCI-2.2 Latency Timer expiration during MWI cycles. csr2xcal_cacheline_size[7:0]
DIS_64BIT_BUS	8	RW	0	0	0: Bus is 64 bits wide 1: Bus is 32 bits wide This bit controls driving REQ64 at release of Reset. Megacell assumes this is the value of REQ64 latched on rising edge of pci_reset. Used to determine PCI(X) 64-bit bus capability. (csr2xcal_64bit_bus_en_n) This bit must be set (by firmware) on port 3.
DIS_ACK64	9	RW	0	0	0: Enable 64-bit Target capability on this port 1: Disable 64-bit Target capability (csr2xcal_64bit_tgt_en_n) This bit must be set (by firmware) on port 3.
DIS_REQ64	10	RW	0	0	0: Enable 64-bit Initiator capability 1: Disable 64-bit Initiator capability (csr2xcal_64bit_initr_en_n) This bit must be set (by firmware) on port 3.
DIS_BURST	11	RW	0	0	0: Enable PCI initiator burst capability. 1: Disable PCI initiator burst capability. (csr2xcal_initr_burst_en_n)
Reserved	14:12	RAZ	0		
EN_IO7_PARK	15	RW	0	0	0: Park GNT on last master 1: Park GNT on IO7
Spl_Cmp_MSG	19:16	RW	0		Split Completion Message. This field is what IO7 will provide in the device specific field of a split completion message.
EN_MSTR_LT	20	RW	0	1	0: follow the PCI spec for master latency (exception: disconnect at cache line boundaries) 1: ignore the master latency timer csr2xcal_lattmr_disable
EN_PCHK	21	RW	0	1	Disables checking parity on AD[63::00] and C/BE[7::0]# during PCI address and data phases. csr2xcal_par_en
Reserved	22	RAZ	0	0	
EN_TLB CACHE	23	RW	0	1	If set TLB entries will be cached coherently. If clear TLB entries will be Fetched and translations discarded after first use. csr2tlb_cache_ena
Reserved	25:24	RAZ	0		

1500

FIG. 10A

Name	Extent	Access	Initial State	Firmware Inited State	
EN_ASSERT_SERR	26	RW	0	0	Enable SERR assertion on PCI(X) bus. csr2p_serr_en This bit has unexpected side effects in the x-caliber core. IO7 will correctly detect and log command/address/attribute parity errors with this bit clear and will target abort the effected transaction. Unwanted side effects of setting this bit include assertion of SERR# when the target of a PIO write asserts PERR#.
Reserved	27	RAZ	0		
RM_TYPE	29:28	RW	01	01	Control the Prefetch algorithm used for PCI memory read multiple command. 00 = two DMA state machines (allows even distribution for a heavily populated bus) 01 = six DMA state machines (default) 10 = eight DMA state machines (for better single stream performance) 11 = eleven DMA state machines (never allow 12 on a read)
DIS_FUNC_ALIAS	30	RW	0	0	0: Allow IO7 to identify itself using multiple function numbers in PCI-X 1: IO7 uses only one function number
EN_AGP_RD_CACHE	31	RW	0	0	This must always be set to 0 on Port 3 0: Disable prefetch data cache (only use Fetch commands) for PCI DMA read data 1: Enable prefetch data cache (use prefetch commands)
EN_PREFETCH	32	RW	0	1	0 = No prefetch; fetch minimum only 1 = Use Prefetch Prediction
Reserved	34:33	RAZ	0	0	
PCI_ARB_MODE	36:35	RW	0	0	0: Round Robin 1: IO7 Priority Mode: IO7 is given the highest priority and is granted the bus whenever it is requested. When IO7 is not requesting the bus it is round robin. 2: Bus hog mode: device 0 ("slot 0") is given highest priority and is granted the bus whenever it is requested. Otherwise it is round robin. Peer to peer is not supported to or from the "bus hog" device. UPE_PCI_22_MODE must be 0 (strict round-robin) when running in Bus Hog mode. 3: reserved
EN_PCI_RD_CACHE	37	RW	0	0	This should be set to 0 on PCI-X and to 1 or 0 on PCI buses. csr2upe_en_rd_cache 0: Disable prefetch data cache (only use Fetch commands) for PCI DMA read data 1: Enable prefetch data cache (use prefetch commands)
UPE_PCI_22_MODE	38	RW	0	0	PCI 2.2 read return (Down hose) ordering compliant mode: csr2upe_pci_22_mode 0 = Strict round-robin (DMA/PPR fills MAY pass PIO/PPR Writes)

~1502

FIG. 15B 10B

Name	Extent	Access	Initial State	Firmware Inited State	
					1 = IO7 Priority mode (2.2 compliant) (DMA/PPR fills **SHALL NOT** pass PIO/PPR Writes)
UPE_ENG_EN<11:0>	50:39	RW	0	FFF	Enable up state machine engines; one bit per engine. Note: When there is peer-to-peer read traffic at least two engines must be enabled. This reservation is to avoid deadlock – writes always make progress. Also note: Port 3 must have at least 4 engines enabled, UPE_ENG_EN<3:0> to support "AGP long reads" and to limit PCI to engines <11:4>. Use this field to cause IO7 DMA to go quiescent in support of hot add or swap of a CPU. csr2upe_eng_en[11:0]
ENA_AGP_ORDER	51	RW	1	1	*This bit effects Port 3 only* 1: Use AGP ordering rules (Up Hose reads may bypass writes) 0: Use PCI ordering rules
UPE_PPRWR_RX	52	RW	0	0	Relax ordering for PPR Writes: 0 – Peer writes are not ordered with respect to other peer writes 1- Peer writes are ordered by limiting to one at a time. csr2upe_pprwr_rx
HPCE_ENA	53	RW	0		Set to enable external hot plug logic.
Reserved	60:54	RAZ	0	0	
AGP_MW	61	RW	0	1	0: SBA48 is Logical "OR" of SBA address bits 47:32 (use Window 3 as 4G Scatter/Gather target) 1: SBA49 always set (AGP uses Monster Window only) csr2agp_mw **Only meaningful on Port 3**
AGP_RD_CONCAT	62	RW	0	1	Enable concatenation of reads from AGP csr2agp_rd_concat **Only meaningful on Port 3**
AGP_WR_CONCAT	63	RW	0	1	Enable concatenation of writes from AGP csr2agp_wr_concat **Only meaningful on Port 3**

~1504

~1501

FIG. ~~15~~ 10C

10C

1600

Name	Extent	Access	Initial State	RW Limited State	
UPH_PID	10:0	RW	x400		PID<9:0> - PID of this device used in all request packets. Note that PID<9> is always set to 1 for IO7. csr2uph_pid[10:0]
UPH_CD_REQ	15:11	RW	0		Up Hose buffer credits: Req csr2mux_crdt_req[4:0]
UPH_CD_RIO	20:16	RW	0		RdIO csr2mux_crdt_rio[4:0]
UPH_CD_WIO	25:21	RW	0		WrIO csr2mux_crdt_wio[4:0]
UPH_CD_BLK	30:26	RW	1		BlkResp csr2mux_crdt_blk[4:0]
UPH_CD_NBK	35:31	RW	1		NoBlk csr2mux_crdt_nbk[4:0]
UPH_FR_CNT	36	RW	0		csr2uph_fr_cnt 0: Force errors as one-shot, single flit ASAP. In this mode the UPH_FR_xxx bit is cleared by hardware after the error is posted. 1: Force errors once every 2^{20} forward clock ticks
UPH_FR_HDR	37	RW	0	•	csr2uph_fr_hdr 0: Force errors on Data flit 1: Force errors on Header flit
UPH_FR_SBE	38	RW	0	•	Force: Single Bit Error csr2uph_fr_sbe
UPH_FR_DBE	39	RW	0		Double Bit Error csr2uph_fr_dbe
UPH_FR_GBG	40	RW	0		Garbage code csr2uph_fr_gbg
UPH_ARB_MODE	42:41	RW	0		Controls priority of AGP relative to other ports. (Port 7 is first because all fwd-misses come through it). 0 – Port 7 first; round robin 0,1,2,3 1 – Port 7 first, Port 3 Second, round robin 0,1,2 2:3 - reserved
Reserved	63:43	RAZ	0		

~ 1602a
~ 1602b
~ 1602c
~ 1602d
~ 1602e

1602

FIG. 11

1700

Name	Extent	Access	Initial State	Firmware Initialized State	
UPE_FLUSH_CACHE	0	W/RAZ	0	0	Set to invalidate all (fetched) non-coherent blocks. VictimClean coherent blocks. Set by write or as a side effect of Fault Reset. This appears the same as a forward hit on all cached data. csr2upe_flush_cache
UPE_CACHE_INV	1	RO	0		Set when one or more blocks in TLB, read and write caches are valid (a pending request, victim or dirty data) NOTE- this may never clear if there is an error. In error case just use PCI_RESET.
Reserved	2	RAZ	0		
PCI_RESET	3	RW	0	1	1: PCI reset not asserted 0: PCI Reset asserted.
Reserved	63:4	RAZ	0		

~1702

~1704

FIG. 17 13

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